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BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER	
RUTZ, JARED IAN	

ART UNIT	PAPER NUMBER
2187	

DATE MAILED: 09/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/811,125	ROSENBLUTH, MARK B.	
	Examiner	Art Unit	
	Jared I. Rutz	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/19/06;7/10/05;3/25/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-24 as amended on 2/4/2005 are pending in the instant application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. **Claims 1-6, 8-13, and 15-22** are rejected under 35 U.S.C. 102(b) as being anticipated by Heddes (US 5,450,351).

4. **Claim 1** is taught by Heddes as:

a. *A content addressable memory, comprising: at least one tag input.* Column 6 lines 5-6 shows that a keyword is applied to the RCAM.

b. *At least one output.* Column 6 lines 12-14 show that the RCAM outputs an N bit word with the matching line set to 1.

c. *At least one random access memory.* Figure 2, discussed at column 5 lines 59-62, shows the use of three RAM blocks.

d. *And circuitry to: perform multiple read operations of the at least one random access memory, different ones of the read operations specifying an address based on different subsets of bits of a tag.* Column 6 lines 5-12 shows

that the keyword is split into subsets, and each subset is applied to one of the RAM blocks.

e. *And based on the multiple read operations, generate at least one signal via the at least one output.* Column 6 lines 12-14 show that an AND operation results in an N bit word that shows the matching line.

5. **Claim 2** is taught by Heddes as:

f. *The content addressable memory of claim 1, wherein the at least one signal comprises at least one signal selected from the following group: a hit signal and an entry number signal.* Column 6 lines 12-14 show that an AND operation results in an N bit word that shows the matching line, which indicates the entry number that matches the input key.

6. **Claim 3** is taught by Heddes as:

g. *The content addressable memory of claim 1, wherein the at least one random access memory comprises multiple random access memories.* Figure 2, discussed at column 5 lines 59-62, shows the use of three RAM blocks.

7. **Claim 4** is taught by Heddes as:

h. *The content addressable memory of claim 3, wherein a number of tag subsets used in the multiple read operations is equal to the number of random*

access memories. Column 6 lines 5-12 shows that the 6 bit keyword is split into three 2 bit subsets, and each subset is applied to one of the RAM blocks.

8. **Claim 5** is taught by Heddes as:

i. *The content addressable memory of claim 4, wherein each of the subsets of bits of the tag forms an address applied to each of the respective random access memories.* Column 6 lines 5-12 shows that the keyword is split into subsets, and each subset is used to address one of the RAM blocks.

9. **Claim 6** is taught by Heddes as:

j. *The content addressable memory of claim 1, wherein the multiple read operations comprise more than one read operation applied to the same random access memory.* Column 6 lines 48-65 teach using a 12 bit keyword which is supplied to the RCAM in two 6 bit portions. A read is made to each of the RAMs for each portion of the keyword.

10. **Claim 8** is taught by Heddes as:

k. *The content addressable memory of claim 1, wherein the circuitry is constructed to perform at least two of the read operations in parallel.* Column 5 line 64 to column 6 line 1 shows that the three sets of output data from the RAMs are bitwise ANDed. As the three sets of output data are combined without any indication of one or more of the sets of output data being stored in any sort of

memory device, it is inherent that the output data from the RAMs are being output in parallel.

11. **Claim 9** is taught by Heddes as:

l. *The content addressable memory of claim 1, wherein the circuitry further comprises circuitry to set bits of the at least one random access memory in response to a tag value to be written to the content addressable memory.* Column 6 lines 15-22 show the use of a control RAM to change bits in the three RAMs to map a matching line to a different keyword.

12. **Claim 10** is taught by Heddes as:

m. *The content addressable memory of claim 9, wherein the tag value to be written comprises a ternary tag value including at least one "don't care" bit and wherein the circuitry to set bits comprises circuitry to set bits for different values of the "don't care" bit.* Column 7 lines 7-14 show that a functional memory device, which is shown at column 1 lines 56-61 is a CAM where single bits can be set to a "don't care" state, is implemented by writing 1 to the second bit of the second word of the first memory at the location addressed by the different values of the "don't care" bit.

13. **Claim 11** is taught by Heddes as:

n. *The content addressable memory of claim 1, wherein the at least one random access memory stores data at each address identifying entries sharing a value of a subset of the bits of the tag.* Column 3 lines 29-32 show that to generate a match at bit I for a keyword, each bit I of the m memory locations corresponding to the m subsets of the keyword has to contain a 1.

14. **Claim 12** is taught by Heddes as:

o. *A content addressable memory, comprising: at least one tag input.* Column 6 lines 5-6 shows that a keyword is applied to the RCAM.

p. *Multiple random access memories, each memory corresponding to a different set of bit positions within a tag.* Column 2 lines 59-63 show that m subsets of the keyword are applied to m RAMs.

q. *Circuitry to: apply different subsets of the bits of the tag as addresses to the different respective random access memories in read operations.* Column 6 lines 5-12 shows that the keyword is split into subsets, and each subset is applied to one of the RAM blocks.

r. *And AND output of the random access memories in response to the read operations.* Column 6 lines 12-14 show that an AND operation results in an N bit word that shows the matching line.

15. **Claim 13** is taught by Heddes as:

s. *The content addressable memory of claim 12, further comprising an encoder to encode the results of the AND.* Column 3 lines 22-27 show that a priority encoder may be used on the matching lines.

16. **Claim 15** is taught by Heddes as:

t. *The content addressable memory of claim 12, wherein the circuitry further comprises circuitry to set at least one bit in each of the multiple random access memories based on a tag value to write.* Column 6 lines 15-22 show the use of a control RAM to change bits in the three RAMs to map a matching line to a different keyword.

17. **Claim 16** is taught by Heddes as:

u. *The content addressable memory of claim 15, wherein the circuitry to set at least one bit comprises circuitry to write multiple bits based on a ternary tag value.* Column 7 lines 7-14 show that a functional memory device, which is shown at column 1 lines 56-61 is a CAM where single bits can be set to a "don't care" state, is implemented by writing 1 to the second bit of the second word of the first memory at the location addressed by the different values of the "don't care" bit.

18. **Claim 17** is taught by Heddes as:

v. *A method, comprising: dividing a received content addressable memory lookup tag value into multiple subtags values; performing multiple read operations of at least one random access memory using addresses based on the multiple, respective, subtag values.* Column 5 lines 59-68 shows that the keyword is split into subsets, and each subset is applied to the address lines of one of the RAM blocks.

w. *And based on the read operations, determining which, if any, entries feature each of the multiple subtags and outputting at least one indication in response to the determining.* Column 5 line 68 to column 6 line 14 show that the data output from the RAMs is ANDed together to produce a N bit word with a 1 where all the data from the RAMs show a 1, which indicates a match at that location.

19. **Claim 18** is taught by Heddes as:

x. *The method of claim 17, wherein performing multiple read operations comprises using each of the multiple subtags as at least a portion of an address specified in the read operations.* Column 5 lines 59-68 shows that the keyword is split into subsets, and each subset is applied to the address lines of one of the RAM blocks.

20. **Claim 19** is taught by Heddes as:

y. *The method of claim 17, wherein the at least one random access memory comprises multiple random access memories.* Figure 2, discussed at column 5 lines 59-62, shows the use of three RAM blocks.

21. **Claim 20** is taught by Heddes as:

z. *The method of claim 19, wherein the multiple random access memories store a bit vector of entry values at subtag addresses.* Column 3 lines 5-19 shows that the RAMs store N bits, each of which indicate if a subset of a keyword provided to the RAM matches a stored keyword at each of I locations.

22. **Claim 21** is taught by Heddes as:

aa. *The method of claim 17, further comprising: receiving a tag to write; and setting bits in the at least one random access memory based on the received tag.* Column 6 lines 15-22 shows that a control RAM can be used to store the keyword to a matching line at the address corresponding to the matching line, and that this stored keyword is used to change the stored bits in the RAMs to change the keyword that corresponds to a matching line.

23. **Claim 22** is taught by Heddes as:

bb. *The method of claim 21, wherein receiving a tag comprises receiving a tag including at least one "don't care" bit; and wherein the setting bits comprises writing entry data associated with multiple values of the same subtag within a*

one of the at least one random access memories. Column 7 lines 7-14 show that a functional memory device, which is shown at column 1 lines 56-61 is a CAM where single bits can be set to a "don't care" state, is implemented by writing 1 to the second bit of the second word of the first memory at the location addressed by the different values of the "don't care" bit.

24. **Claims 1, and 6-7** are rejected under 35 U.S.C. 102(b) as being anticipated by Edgar (US 5,806,083).

25. **Claim 1** is taught by Edgar as:

cc. *A content addressable memory, comprising: at least one tag input.* Column 8 lines 47-49 shows that an input entity is stored in register 109 of figure 5 which is coupled to bus 104 of figure 5.

dd. *At least one output*. Column 11 lines 23-27 shows that the final match information is output on bus 107 of figure 5.

ee. *At least one random access memory*. RAM 120 of figure 5.

ff. *And circuitry to: perform multiple read operations of the at least one random access memory, different ones of the read operations specifying an address based on different subsets of bits of a tag*. Column 9 lines 34-37 shows that the RAM 120 is read once per cycle in a sequence determined by the 3 bit control signal. Column 8 lines 50-61 shows that there are 6 cycles to correspond to the six 8 bit slices of the 48 bit input data entity.

gg. *And based on the multiple read operations, generate at least one signal via the at least one output.* Column 11 lines 18-27 shows that the final mask signal is the final ANDed signal of match information and is output on bus 107 in the last cycle.

26. **Claim 6** is taught by Edgar as:

hh. *The content addressable memory of claim 1, wherein the multiple read operations comprise more than one read operation applied to the same random access memory.* Column 9 lines 34-37 shows that the RAM 120 is read once per cycle in a sequence determined by the 3 bit control signal. Column 8 lines 50-61 shows that there are 6 cycles to correspond to the six 8 bit slices of the 48 bit input data entity.

27. **Claim 7** is taught by Edgar as:

ii. *The content addressable memory of claim 6, wherein individual ones of the more than one read operations applied to the same random access memory specify an address based on a subset of the tag value and an identifier of a section of the random access memory.* Column 8 lines 50-61 shows that there are 6 cycles to correspond to the six 8 bit slices of the 48 bit input data entity. Column 9 lines 4-5 show that the 3 bit signal defines the location section of the RAM.

Claim Rejections - 35 USC § 103

28. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

29. **Claim 14** is rejected under 35 U.S.C. 103(a) as being unpatentable over Heddes (cited *supra*) in view of McKenzie et al. (US 2004/0139275).

30. **Claim 14** is taught by Heddes as shown supra with respect to claim 13.

31. Heddes does not expressly disclose that a priority encoder contains a network of at least one OR gate.

32. With respect to Claim 14, McKenzie teaches:

jj. *The content addressable memory of claim 13, wherein the circuitry to encode the results comprises at least one selected from the following group: a network of at least one OR gate to operate on the results of the AND-ing, and a one-hot to binary encoder.* Figure 9 shows a schematic of a column priority circuit from the priority encoder of figure 5. Figure 9 contains OR gates 536, 538, 244, and 550.

33. Heddes and McKenzie are analogous art because they are from the same field of endeavor, the design of circuits to key matching.

34. At the time of the invention it would have been obvious to use a priority encoder as taught by McKenzie with the RCAM of Heddes.

35. The motivation for doing so would have been to use a priority encoder that is easily implemented using standard cells of circuitry, McKenzie paragraph 0035.

36. Therefore, it would have been obvious to combine McKenzie with Heddes to obtain the invention as specified in claim 14.

37. **Claims 23-24** are rejected under 35 U.S.C. 103(a) as being unpatentable over Morrison (US 2003/0235194) in view of Edgar (cited *supra*).

38. **Claim 23** is taught by Morrison as:

kk. *A network forwarding device, comprising: a switch fabric.* Figure 6 item 104.

ll. *And multiple line cards interconnected by the switch fabric.* Figure 6 items 102 A, 102 B, and 102 C.

mm. *Individual ones of the line cards comprising: at least one network port.* Figure 6 item 116.

nn. *And circuitry to process packets received via the at least one port.* Figure 6 items 118 and 120.

oo. *The digital logic circuitry including a content addressable memory.* Paragraph 0038 shows that memory 120 may be a CAM.

39. Morrison does not expressly disclose the claimed CAM.

40. with respect to claim 23, Edgar teaches:

pp. *The content addressable memory comprising: at least one tag input.* Column 8 lines 47-49 shows that an input entity is stored in register 109 of figure 5 which is coupled to bus 104 of figure 5.

qq. *At least one output.* Column 11 lines 23-27 shows that the final match information is output on bus 107 of figure 5.

rr. *At least one random access memory.* RAM 120 of figure 5.

ss. *Content addressable memory circuitry to: perform multiple read operations of the at least one random access memory, different ones of the read operations specifying an address based on different subsets of the bits of a tag.* Column 9 lines 34-37 shows that the RAM 120 is read once per cycle in a sequence determined by the 3 bit control signal. Column 8 lines 50-61 shows that there are 6 cycles to correspond to the six 8 bit slices of the 48 bit input data entity.

tt. *And based on the multiple read operations, generate at least one signal via the at least one output.* Column 11 lines 18-27 shows that the final mask signal is the final ANDed signal of match information and is output on bus 107 in the last cycle.

41. Morrison and Edgar are analogous art because they are from the same field of endeavor, the design of network devices.

42. At the time of the invention it would have been obvious to use the improved Cam of Edgar in the line cards of Morrison.

43. The motivation for doing so would have been to use a CAM that requires less circuit area, Edgar column 2 lines 12-19.

44. Therefore, it would have been obvious to combine Edgar with Morrison for the benefit of reduced circuit area to obtain the invention as specified in **claims 23 and 24**.

45. **Claim 24** is taught by Morrison as:

uu. *The network forwarding device of claim 23, wherein at least one of the line cards comprises a network processor having multiple multi-threaded engines integrated on a single die*. Paragraph 0017.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jared I. Rutz whose telephone number is (571) 272-5535. The examiner can normally be reached on M-F 8:00 AM - 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Brian R. Peugh
Primary Examiner
9/13/06

Jared I Rutz
Examiner
Art Unit 2187

jir